Deekshith Anantha

Raleigh, NC
+1(984) 382-1068 | ananthadeekshith@gmail.com | linkedin.com/in/deekshith-anantha
Github | Deekshith Anantha

EDUCATION

North Carolina State University **Aug 2025 - May 2027**
Master of Science (MS), Computer Engineering (GPA: 4.00/4.00)
- **Coursework:** Object-Oriented Design and Development, Compiler Optimization and Scheduling, Microprocessor Architecture, Embedded Systems Architecture, Advanced Microarchitecture, Architecture of Parallel Computers

RV College of Engineering **Aug 2019 - Jun 2023**
Bachelor of Engineering, Electronics and Telecommunication (GPA: 7.9/10)

WORK EXPERIENCE

AIRBUS | *Software Development Engineer* **Jul 2023 - Jul 2025**
Contributed to the development of firmware for the Flight Warning Computer on Next-Gen Single Aisle Aircraft (A320s), demonstrating C/C++ and embedded systems expertise.
- Integrated hardware-software components, conducted requirement-based testing, and performed real-test bench debugging using **Trace32** and **GDB**, solidifying rigorous firmware testing and debugging practices
- Ensured compliance and software reliability through static analysis of the Flight Warning application using the Astrée tool, leading to enhanced system performance
- Engineered a **CI/CD** pipeline leveraging Jenkins, achieving a **50**% reduction in build and deployment time and substantially optimizing the development workflow.
- Integrated the SDAC (System Data Acquisition Concentrator) test bench configuration with the Flight Warning Computer by introducing a Lua-based graphical user interface, mitigating resource constraints, and increasing productivity by **30%.**
- Automated the migration of 34 software components to the latest Airbus toolchain using Python and Shell scripting, cutting migration **time by 80%**.
- Optimized the cockpit simulation by eliminating over **15,000** signals using Python scripts, resulting in a **15%** increase in computational efficiency for the Flight Warning Computer.

AIRBUS | *Engineering Intern* **Mar 2023 - Jul 2023**
Developed an auto-process tool to streamline the Change and Configuration Management process, aligning with systematic firmware documentation practices.
- Gained hands-on experience in embedded systems by developing **DO-178C**-compliant automation projects using Python, reinforcing proficiency in scripting for testing and debugging.
- Implemented efficient workflows using **Agile** and **CI/CD** practices that significantly improved team productivity and optimized development cycles, reducing the release time of features.

PROJECTS

Course Enrollment & Feedback System (Ruby on Rails, RSpec)
- Developed a full-stack web application in **Ruby on Rails** to manage university course registration, student feedback, and administration. Implemented a secure, role-based authentication system for **Student** and **Admin** users with distinct permissions and data access controls. Engineered core enrollment logic to manage course capacity and automated waitlists, triggering cascading updates on student drops or deletions. Ensured code reliability and data integrity by writing unit tests for models and controllers using **RSpec**.

Cache and Memory Hierarchy Design (C++)
- Implementation of generic cache memory with two levels, utilizing LRU and WBWA policy. Stream buffers at different levels were incorporated to enable prefetching and to minimize the memory access. Analyzed the implementation for various configurations of associativity, block size, and extracted performance metrics like miss rate, memory traffic, and access time.

Money Manager: Personal Finance Platform
- Built a robust REST API using FastAPI, MongoDB, and JWT based authentication with > 95% test coverage. Developed a Telegram bot frontend with extensibility to Discord and web platforms. Key features include cloud sync, receipt scanning, global currency support, and its fully cusomizable.

Dynamic Instruction Scheduling Simulator (C++)
- Designed an out-of-order processor with super scalar bandwidth of N instructions that precisely calculates the cycles for a given trace.
- Utilizing register renaming, WAR and WAW hazards were eliminated. Analyzed variations in IPC for various configurations of super scalar widths, scheduler queue size, and Reorder buffer size.

Technical Skills

- **Additional Skills:** AWS, Agile, Bash, Blockchain, C/C++, CI/CD, Canva, Confluence, Consul, Data Analysis, Data Science, Data Structures & Algorithms, Development Operations (DevOps), Digital Ocean, Docker, MS Office, Git, GCP, GoLang, GraphQL, Groovy, gRPC, HTML/CSS, Heroku, JIRA, JavaScript, Jupyter, Linux/Unix, MySQL, Nginx, NodeJS, NoSQL, Openstack, Pandas, Postman, Prometheus, PyTest, Python, R, RDBMS, React, Ruby, Ruby on Rails, SCRUM, SQL, Selenium, TCP/IP, TDD, Tailwind CSS, Wireshark.